REMARKS

The above amendments and following remarks attend to each and every rejection and objection presented in the pending February 23, 2005 office action. Claims 1 and 2 are amended for clarity. No new matter is added. Claims 1-15 remain pending, with claims 1, 4, 9, 10 and 15 being independent.

Claim Objections

Claim 1 is objected to because of informalities. The Examiner requests clarification of the phrase "storing a cumulative value of a design element characteristic." Claim 1 is thus amended to separate the step of "storing a cumulative value" into two steps of "summing a cumulative design element characteristic value" and storing the cumulative design element characteristic value," thereby clarifying that the cumulative value represents a summed characteristic of the design elements that are connected to a specific node in the circuit. Claim 2 is also amended to clarify the cumulative design element characteristic value is stored in a hash table. Support for these amendments can be found in at least paragraphs [0009-0011] of the specification. No new matter is added.

Reconsideration is respectfully requested.

Claim Rejections – 35 U.S.C. § 103

Claims 1-3 stand rejected under 35 U.S.C. §103(a) as being obvious over U.S. Patent Application No. 5,949,691 granted to Kurosaka et al. (hereinafter Kurosaka). Respectfully we disagree.

For the purpose of the following discussion, the Examiner is respectfully reminded of basic considerations which apply to obviousness rejections.

When applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:

(A) The claimed invention must be considered as a whole;

(B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;

(C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and

(D) Reasonable expectation of success is the standard with which obviousness is determined. MPEP §2141.01, *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1134 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

It is thus noted that to substantiate a *prima facie* case of obviousness, the initial burden rests with the Examiner who must fulfill three requirements:

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings.

Second, there must be a reasonable expectation of success.

Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The ***teaching or suggestion*** to make the claimed combination **and** the ***reasonable expectation of success*** **must** ***both be found in the prior art,*** **and not** ***based on applicant's disclosure***. (emphasis and formatting added) MPEP § 2143, *In re vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

Amended claim 1 recites a method for determining unmatched design elements in a circuit including the steps of:

a) determining instances of a first type and a second type of the design elements that are connected to a specific node in the circuit;

b) storing a gate signal name for each determined said instance of the first type of design element in a first list;

c) storing the gate signal name for each determined said instance of the second type of design element in a second list;

d) determining a cumulative design element characteristic value by summing a design element characteristic for each determined said instance of the first and the second types of the design elements;

e) storing the cumulative design element characteristic value in association with the gate signal name;

f) performing a set difference operation on the first list and the second list to determine orphan gate signal names that appear in either one of the lists but not in both; and

g) determining a cumulative value for said design element characteristic, by summing the design element characteristic value corresponding to each said

first type of design element gate signal name that matches one of said orphan gate signal names, to produce a total design element characteristic value.

Kurosaka discloses a method and a logic circuit verification device for verifying logic circuit equivalence. Kurosaka identifies points within a circuit that correspond to one another using a technique for matching identical signal names or non-identical signal name associated with these points, based upon corresponding rules. See at least Kurosaka col. 7, lines 10-35. Using the identified points within the circuit, Kurosaka partitions the circuit unto sub-circuits that are then checked for equivalence. See at least Kurosaka col. 8, lines 34-50. Kurosaka thus has no need to sum characteristics or determine orphaned signals.

Kurosaka does not disclose or suggest determining instances of a first type and a second type of design elements that are connected to a specific node in the circuit as required by step a) of claim 1. Kurosaka does not disclose or suggest creating two lists of first type and second type of design elements as required by steps b) and c). Kurosaka does not disclose or suggest determining cumulative design element characteristic value by summing a design element characteristic for each determined instance of the first and the second types of the design elements as required by step d). Kurosaka does not disclose or suggest storing the cumulative design element characteristic value in association with the gate signal name as required by step e). Kurosaka does not disclose or suggest performing a set difference operation on the first list and the second list to determine orphan gate signal names that appear in either one of the lists but not in both as required by step f). Kurosaka does not disclose or suggest determining a cumulative value for the design element characteristic, by summing the design element characteristic value corresponding to each the first type of design element gate signal name that matches one of the orphan gate signal names, to produce a total design element characteristic value, as required by step g).

Since the goals of Kurosaka are to identify equivalent circuits within the design and to determine if these circuits are equivalent, there would be no desire to identify orphaned gate signal names or to sum design element characteristics in Kurosaka. Kurosaka cannot therefore render claim 1 obvious. Reconsideration of claim 1 is respectfully requested.

Claims 2 and 3 depend from claim 1 and benefit from like argument. However, these claims have additional features that patentably distinguish over Kurosaka. For example amended claim 2 recites the cumulative design element characteristic value for each determined said instance of the first and the second types of the design elements is stored in a hash table. Kurosaka does not disclose or suggest storing a cumulative value within a hash table. Claim 3 recites the first and the second types of the design elements are selected from a family of design elements consisting of transistors, wires, capacitors, resistors, and power sources. Kurosaka does not disclose or suggest design elements consisting of transistors, wires, capacitors, resistors, and power sources.

Reconsideration of claims 1-3 is respectfully requested.

We thank the Examiner for indicating allowable subject matter of claims 4-15.

In view of the above arguments, we contend that claims 1-15 are allowable and respectfully request reconsideration.

It is believed that no fees are due in connection with this amendment. If any fee is due, please charge Deposit Account No. 08-2025.

Respectfully submitted,

By: _____

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